Slavica Malobabic
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## EDUCATION

• **PhD studies in Electrical Engineering – Presidential Fellowship** University of Central Florida (UCF), GPA 4 / 4, Advisor: Dr. Juin J. Liou. Started Fall 2006. Expected graduation date December 2010.

• **Master's studies, Major Solid State Electronics,** GPA 5 / 5, top 5% of graduating class Simon Bolivar University (USB), Caracas, Venezuela, October 2006. Advisor: Dr. Adelmo Ortiz – Conde.

• **Professional Electronics Engineer Degree** (5 year program), GPA 4.69 / 5, top 5% of graduating class, USB, January 2005. Advisor: Dr. Adelmo Ortiz – Conde.

## EXPERIENCE

• **Research assistant,** University of Central Florida UCF and Analog Devices as part of long term project: "Failure criteria metric under ESD stress conditions" with University of Central Florida. Topics: Device simulation in DC and ESD regime, Gate oxide breakdown characterization and modeling and Development of design guidelines and failure metrics under Human Body Model (HBM) and Human Metal Model (HMM) type stresses for ESD structures and DMOS. Software: Synopsys, Sentaurus tools. Instruments: TLP, vfTLP tester, Keithley 4200, Hanwa HMM tester. June 2007 –

• **Research assistant,** UCF and Intersil -Device simulation and device simulator calibration and HHNEC - Process simulation. Software: Silvaco: Atlas, Athena. Instruments: device characterization and measurement. August 2006 – February 2007

• **Research Assistant** USB, Physics based modeling and simulation of emerging devices (SOI and Double gate (DG) MOSFETs). Software: Maple, Sigmaplot, Comsol. April 2005 – July 2006

• **Teaching Assistant** Solid State Electronics, USB, Sep-Dec 2004

## PUBLICATIONS

1) S. Malobabic, A. Ortiz-Conde, F. J. García Sánchez, "Modeling the Undoped-Body Symmetric Dual-Gate MOSFET", 5th IEEE Int. Caracas Conf. on Cir. Dev. and Sys., (Dominican Republic), pp. 19 -25, Nov. 2004

2) A. Ortiz-Conde, F. J. García Sánchez, S. Malobabic, J. Muci, “Analytic Solution for the drain current of Undoped Symmetric Dual-Gate MOSFETs (Invited)", 2005 Workshop on Compact Modeling (WCM), Anaheim, California, U.S.A, May 2005. See also: http://www.nsti.org/Nanotech2005/WCM2005/

3) A. Ortiz-Conde, F. J. García Sánchez, S. Malobabic “Analytic Solution of the Channel Potential in Undoped Symmetric Dual-Gate MOSFETs", IEEE transactions on Electron Devices, vol. 52, no. 7, pp. 1669 – 1672, July 2005

4) A. Ortiz-Conde, E. Miranda, F. J. García Sanchéz, E. Farkas, and S. Malobabic. “Modeling the Post-Breakdown Current in MOS devices on p-silicon substrate”, IEEE Int. Caribbean Conf. on Cir. Dev. and Sys., 2006

5) A. Ortiz-Conde, F. J. García Sánchez, J. Muci, and S. Malobabic. “A General Analytical solution to the One-Dimensional Undoped Oxide-Silicon-Oxide System”, IEEE Int. Caribbean Conf. on Cir. Dev. and Sys., 2006

6) A. Ortiz-Conde, F. J. García Sánchez, Slavica Malobabic, J. Muci, R Salazar, “Double-Gate MOSFET (invited) ”, 8th International Conference on Solid-State and Integrated-Circuit Technology, October 23-26, 2006, Shanghai, China.

7) F. J. García Sánchez, A. Ortiz-Conde, S. Malobabic, “Applications of Lambert’s Function in Electronics”, Universidad. Ciencia y Tecnología (UCT), Nº 41, December 2006.

8) A. Ortiz-Conde, F. J. García-Sánchez, J. Muci, S. Malobabic, J. J. Liou, “A Review of Core Compact Models for Undoped Double-Gate SOI MOSFETs ”, IEEE transactions on Electron Devices, vol. 54,no 1,pp. 131-140, January 2007.

9) S. Malobabic, D. F. Ellis, J.A Salcedo, Y. Zhou; J.-J Hajjar, J.J. Liou, “ Gate oxide evaluation under very fast transmission line pulse (VFTLP) CDM-type stress” , IEEE Int. Caribbean Conf. on Cir. Dev. and Sys., 2008

10) D. F. Ellis, S. Malobabic, “Prediction of Gate Dielectric Breakdown in the CDM Timescale Utilizing Very Fast Transmission Line Pulsing”, International Reliability Physics Symposium (IRPS) April, 2009

11) S. Malobabic, D. F. Ellis, J.A Salcedo, Y. Zhou; J.-J Hajjar, J.J. Liou, “Very Fast Transient Simulation and Measurement Methodology for ESD Technology Development”, IRPS April, 2009

12) J. J. Liou, S. Malobabic, D. F Ellis, J. A. Salcedo, J.-J Hajjar, Y. Zhou “Transient Safe Operating Area (TSOA) Definition for ESD Applications (invited)”, EOS/ESD Symposium ,September 2009.

13) S. Malobabic, J. A. Salcedo, A. W. Righter, J.-J Hajjar, J. J. Liou, “A New ESD Design Methodology for High Voltage DMOS Applications”, EOS/ESD Symposium October 2010.

14) S. Malobabic, J. A. Salcedo, J.-J Hajjar, J. J. Liou, “Analysis of Safe Operating Area of NLDMOS and PLDMOS Transistors Subject to Transient Stresses”, IEEE Transactions on Electron Devices, vol. 57, no. 10, October 2010.

## IEEE POSITIONS HELD

September 2007- May 2010 Chapters’ Chair in Orlando section

Jan 2007- IEEE Electron Device Society Chapter Chair in Orlando Section

Jan – Dec 2007 Components, Packaging, and Manufacturing Technology Chapter Chair in Orlando Section

## IEEE VOLUNTEER WORK

July 2007- April 2008 Registration Committee Chair for 7th IEEE International Caribbean Conference on Devices, Circuits and Systems , April 28th to 30th , 2008, Cancun, Mexico

Sep 2004 Logistics support for 4th Venezuelan Electrical Engineering Congress, Simón Bolívar University, organized by IEEE and Simón Bolívar University, September 7th to 10th ,2004

Jan – Dec 2004 Member of Publications Committee of the 5th *IEEE* International Caracas Conference on Devices, Circuits and Systems, Punta Cana, Dominican Republic, November 3rd to 5th ,2004 (visit: http://pancho.labc.usb.ve/iccdcs2004 )

Feb – May 2002 Member of Publications Committee of the 4th *IEEE* International Caracas Conference on Devices, Circuits and Systems ,Oranjestad, Aruba, Dutch Caribbean, April 17th to 19th ,2002

## HONORS

IEEE Electron Devices Society's 2005 Region 9 Outstanding Student Paper, Honorific mention in undergraduate project and in Master's thesis. IEEE EDS 2008 chapter of the year award. 2009 IRPS best paper award